

Input stage resistant against negative voltage swings

5 The present invention relates to input stages having protection against negative voltage swings. In particular, the present invention relates to CMOS input stages and their protection.

 While modern CMOS IC (complementary metal oxide semiconductor integrated circuit) fabrication technologies are going down with critical geometrical dimensions, the maximum allowed voltage swing across individual transistors and with
10 it the maximum allowed supply voltage is going down rapidly. On the other hand, the signal swing at an input port of a CMOS device may go beyond these voltage limits. Even more problematic is the fact that there are applications where input signals with a negative voltage swing may occur.

15 A CMOS device typically comprises some kind of a level shifter 5, as illustrated in Fig. 1, in order to shift the voltages at the input pad 1 to the lower levels of the V_{DD} voltage domain of the core 6 of the CMOS device. Such a level shifter 5, however, is not suited to handle input signals with a negative voltage swing.

 CMOS ICs have to be protected against electrostatic discharge (ESD) in
20 order to make sure that the circuit is not damaged by voltage peaks. Usually, ESD (ESD) protection elements, such as diodes 2 and 3 are provided between the circuit's input pad 1, the voltage supply terminal V_{DD} and ground GND, as depicted in Fig. 1. ESD protection is employed in order to prevent the very sensitive level shifter 5 from being destroyed when it is subjected to a discharge event. This might happen for
25 example when somebody induces a voltage peak into the circuitry by touching the pins of the chip. Such an ESD protection scheme does not function when negative voltages are applied to the input pad 1, since the diode 3 would enter conduction, which would lead to a clipping of the input signal.

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More details about ESD protection and level shifting for CMOS devices

handling input signals with positive signal swings are addressed in the co-pending patent application entitled "INPUT STAGE RESISTANT AGAINST HIGH VOLTAGE SWINGS", as filed on 06.02.2002 Application number EP02002681.1 was assigned to this co-pending application.

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It is an object of the present invention to provide input stages that are able to handle negative voltage swings and to provide apparatus based thereon.

It is another object of the present invention to provide input stages that are able to handle negative voltage swings and to withstand ESD events, and to provide apparatus based thereon.

These and other objects are accomplished by an apparatus circuit according to claim 1. Further advantageous implementations are claimed in claims 2 – 9.

The present invention allows to realize circuits with reduced fabrication technology costs and less complex system design.

For a more complete description of the present invention and for further objects and advantages thereof, reference is made to the following description, taken in conjunction with the accompanying drawings, in which:

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Fig. 1 is a schematic representation of a conventional CMOS device with ESD protection and level shifter;

Fig. 2 is a schematic representation of a first embodiment of the present invention;

Fig. 3 is a diagram showing the various signals in an apparatus according to the present invention;

Fig. 4 is a schematic representation of a second embodiment of the present invention;

Fig. 5 is a schematic representation of a third embodiment of the present invention;

Fig. 6 is a diagram showing the various signals in an apparatus according

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to the present invention;

Fig. 7 is a schematic representation of a fourth embodiment of the present invention;

Fig. 8 is a schematic representation of a fifth embodiment of the present invention;

Fig. 9 is a schematic representation of an ESD protection scheme, according to the present invention.

10 A first embodiment of the present invention is illustrated in Figure 2. In this Figure, an input stage 10, according to the present invention is shown. It comprises a level shifter 15 being connectable to a signal input 1. The input stage 10 receives an input signal $s(t)$ with a negative signal swing. Since the subsequent circuits, herein referred to as core, are not able to handle negative signals at all, the level shifter 15 provides for a DC shift of said input signal $s(t)$ in order to provide an output signal $r(t)$ with positive signal swing only. As illustrated in Fig. 2, the level shifter 15 comprises an amplifier 17 having a first input 11, a second input 12, and an output 13. The amplifier 17 is part of a network comprising a first capacitor C1, a second capacitor C2, and a transistor 14 serving as a switch. Preferably, the transistor 14 is an n-channel MOS transistor. The first capacitor C1 is arranged between the signal input 1 and the amplifier's first input 11. The second capacitor C2 is arranged in a feedback-loop 18 between the output 13 and the first input 11. There is a reference voltage supply 16 that applies a reference voltage V_{ref} to the amplifier's second input 12.

25 The transistor 14 is arranged in a branch 19 that bridges the second capacitor C2. When applying a high level control signal CNTRL to the gate 14.1 of the transistor 14, the level shifter 15 is initialized or reset. The reset is typically performed each time before an input signal $s(t)$ is applied to the input 1.

30 Whenever the switch 14.1 is closed, the amplifier 17 acts as a unity-gain voltage follower of reference voltage 16, so the output 13 and the input 11 are set close to V_{ref} . Thus the capacitor C1 is charged to $V_{ref} - s(t)$ and DC-level shifting of the input is achieved. As soon as the switch 14.1 is opened, the amplifier 17 together with C1 and C2 acts as an inverting amplifier with a gain of $-C1/C2$.

One may for instance, set the control signal CNTRL to high and release it at the time t_0 , right before the input signal $s(t)$ is applied. After t_0 the output signal $r(t)$ is given by:

$$r(t) = -\frac{C1}{C2} \cdot (s(t) - s(t)|_{t=t_0}) + V_{ref} \quad (1)$$

5 This equation (1) shows that the DC shift provided by the input stage 10 can be determined by the reference voltage V_{ref} and by the ratio of $C1$ and $C2$. This gives arbitrary freedom to accommodate any input voltage swing. The control signal CNTRL is activated from time to time or whenever needed, in order to compensate for a potential discharge of the capacitor $C1$. The discharging occurs due to inevitable
10 leakage currents.

For devices that are made using deep submicron processes, it is important that none of the devices' transistors is subjected to destructive voltages across their terminals. According to the present invention, a high voltage is only carried on the capacitor $C1$, which should be constructed out of available layers, like metal
15 interconnect sandwich structures, or fringe capacitors, which are able to withstand higher voltages.

Fig. 3 shows an example for a constant reference voltage $V_{ref}=1V$ and a sine wave $s(t)$ at the input 1 with a swing between 0V and -4V. The amplifier 17 has a gain of 0.5. At the time $t=t_0$, the control signal CNTRL is released. This signal is
20 released shortly before the signal $s(t)$ is applied to the input 1. The sine wave $s(t)$ starts to oscillate between 0V and -4V. According to the present invention, the output signal $r(t)$ is DC shifted. In the present example, the output signal $r(t)$ oscillates around +1V and has an amplitude of 1V. The output signal $r(t)$ does not enter the negative voltage regime.

25 The device 10 can be modified by adding additional capacitors and switches in order to allow the DC shift to be adjusted, according to current needs. Further details will be given in connection with another embodiment.

Another embodiment, according to the present invention, is depicted in Fig. 4. An apparatus 20 is shown in Fig. 4 that comprises a level shifter 10, or another
30 level shifter according to the present invention, and a bias current source 21. The current source 21 comprises a network having a plurality of PMOS transistors P1, P2, P3, resistors R1 and R2, and a reference current source 22. The current source 21 is

constructed with a current mirror comprising the transistors P1 and P2 connected to a supply voltage node 23. A supply voltage V_{supply} is applied to this node 23. As stated above, in a deep submicron fabrication process the voltage across the terminals of individual transistors must not go beyond the maximum specified voltage V_{max} , which
 5 generally is close to V_{supply} . This would mean that the transistor P2 would be biased beyond the allowed operation range when its source is directly connected to the input node IN. To prevent destruction of the transistor P2, a special cascode transistor P3 is added, which absorbs any voltage beyond V_{supply} , if the input signal $s(t)$ at the node IN goes below 0V. The two resistors R1 and R2 serve as resistive divider controlling
 10 the gate of the cascode transistor P3 depending on the input voltage $s(t)$. If required, additional cascode transistors can be put in series with the cascode transistor P3 to allow for a higher protection range. In this way the voltage between the node 23 and the node 24 is kept below V_{supply} .

The current source 21 is designed so that itself is protected against
 15 negative input voltages.

If V_{tp} is the threshold voltage of the transistor P3 and $s(IN_{min})$ the minimum voltage at the input node IN, the resistive divider is dimensioned to be:

$$-s(IN_{min}) = \frac{R1 + R2}{R2} \cdot V_{tp} \quad (2)$$

Many applications require a bias current source, preferably on chip. A
 20 typical example is a sensor for measuring the power of an RF connection like an antenna. A respective embodiment is illustrated in Fig. 5. In this Figure, an apparatus 30 is illustrated. It comprises a level shifter 10 or 15, or another level shifter according to the present invention, and a bias current source 21 like the one depicted in Fig. 4. The apparatus 30 serves as peak detector for a radio frequency signal RF. At the input
 25 side, there is a network comprising two capacitors C3 and C4, a resistor R, and a diode D. An RF signal is applied to an RF node 31. The current source 21 is designed such that the diode D is properly biased.

Fig. 6 shows an example for a constant reference voltage and an RF voltage at the input 31 with a swing between 2V and -2V. At the time $t=t_0$, the control
 30 signal CNTRL is released. This control signal CNTRL is released shortly before the RF signal is applied to the input 31. The RF signal starts to oscillate between 2V and -2V. Fig. 6 shows the biasing of the diode D at about $t=t_0$, and the transformation of a

negative voltage $s(t)$ to a positive voltage $r(t)$. In Fig. 6, the voltage $x(t)$ at the node 24 (between the transistors P2 and P3) is shown. While the voltage $s(t)$ goes below 0V, the voltage $x(t)$ at node 24 stays within the safe range. This is, the transistor P3 is activated, as desired.

5 According to the present invention, the output signal $r(t)$ is DC shifted. In the present example, the output signal $r(t)$ does not enter the negative voltage regime.

Yet another embodiment, according to the present invention, is depicted in Fig. 7. In Fig. 7, an apparatus 70 is illustrated where the reference voltage V_{ref} and the ratio $C1/C2$ can be changed. In this Figure, an input stage is shown. It comprises a level shifter 75 being connectable to a signal input 71. The input stage receives an input
10 signal $s(t)$ with a negative signal swing. Since the subsequent circuits (not illustrated in Fig. 7) are not able to handle negative signals at all, the level shifter 75 provides for a DC shift of said input signal $s(t)$ in order to provide an output signal $r(t)$ at an output 73 with positive signal swing only. As illustrated in Fig. 7, the level shifter 75 comprises
15 an amplifier 77 having a first input 61, a second input 62, and an output 73. The amplifier 77 is part of a network comprising a first capacitor $C1$, an array of n second capacitors $C2A$, $C2B$ through $C2n$, and a transistor 74 serving as a switch (nsw). Preferably, the transistor 74 is an n-channel MOS transistor. The first capacitor $C1$ is arranged between the signal input 71 and the amplifier's first input 61. The second
20 capacitors $C2A$, $C2B$ through $C2n$ are arranged in a feedback-loop between the output 73 and the first input 61. A reference voltage V_{ref} is supplied by a controller 78 and a digital-to-analog (DAC) converter 79 to the amplifier's second input 62. The output voltage $r(t)$ at the output 73 is measured with an analog-to-digital converter (ADC) 80 and fed as digital data (Adata) to the controller 78. The controller 78 is a digital
25 controller which sets the reference voltage V_{ref} at the input 62 with the aid of the digital-to-analog (DAC) converter 79. Furthermore, the controller 78 tunes the gain of the amplifier 77 by switching the capacitors $C2B$ to $C2n$ in parallel to $C2A$. If the switching signal sb is applied, the second capacitance $C2$ is defined by a parallel arrangement of $C2A$ and $C2B$, for example. That is, $C2 = C2A + C2B$. In this case, the
30 output signal $r(t)$ is given by the equation (3):

$$r(t) = -\frac{C1}{C2A + C2B} \cdot (s(t) - s(t)|_{t=t_0}) + V_{ref} \quad (3)$$

The gain is determined by:

$$gain = \frac{C1}{C2A + \sum_{i=B}^n (C2i \cdot ai)} \quad (4)$$

with $ai=1$, when the switch s is closed and $ai=0$, when the switch s is open. Like the apparatus described before, from time to time a reset is required, since the capacitors $C1$, and $C2A$ to $C2n$ get discharged due to leakage currents.

5 It is also possible to employ a programmable array of capacitors instead of the single first capacitor $C1$.

A block diagram of an apparatus 90 similar to the one depicted in Fig. 7, is given in Fig. 8. The apparatus 90 comprises an input pad 91 where a signal $s(t)$ with negative signal swing is applied. An ESD protection 92 is provided in order to prevent the core against all possible ESD overstress situations. A bias current source 93, similar to the one illustrated in Fig. 4 is provided. A level shifter 95 provides for a DC shift of the signal $s(t)$ at its input 91. A timing circuit 94 provides a control signal CNTRL in order to reset the circuit from time to time. A reference voltage V_{ref} is provided by a reference voltage source 97. The gain of an amplifier inside the level shifter 95 and the reference voltage V_{ref} may be controlled and adjusted by a controller 96, similar to the one illustrated in Fig. 7. The output 91 is connected to a circuit core which is not illustrated in Fig. 8.

The general ESD protection scheme, applied in connection with the present invention, is schematically illustrated in Fig. 9. There are two diodes DP1 and DP2 that are arranged to protect the level shifter and core 103. The diode DP2 is situated between the input node 91 and the supply node 101 and the diode DP1 is situated between the supply node 101 and the substrate 102. A clamp diode DCL1 is situated between the supply node 101 and the substrate 102. The diodes used must be robust enough to withstand the wanted ESD level. Preferably, the diode DP1 comprises an Nwell layer inside a P-epitaxy or P-well layer. The Nwell to substrate 102 breakdown voltage is preferably greater than 20V, for example. The diode DP2 comprises a p+ active region inside the Nwell that also builds the diode DP1. The breakdown voltage of the diode DP2 is preferably greater than 12V. The power protection clamp diode DCL1 limits the voltage on the supply node 101. The limit may be set to be 11V, for example. The resulting voltage range for the input node 91 is therefore 12V to $V_{supply} + V_f$ (diode forward voltage), with the restriction that V_{supply}

$<V_{br}$ (the breakdown voltage of the diode DCL1). Preferably, a protection resistor R_p is situated at the input of the level shifter and core 103, as illustrated in Fig. 9.

For multi power domains, each domain must have such a combination of a P type diode D1 and power clamp diode DCL1.

5 In addition to the protection scheme illustrated in Fig. 9, it is advantageous to employ a so-called secondary protection scheme in order to protect the elements of the level shifter and core. Two different cases are dealt with in the following:

1. If the core is a PMOS drain, this drain must be protected against
10 electrical overstress. This can be done by means of a protection resistor. This resistor is to be calculated to prevent the maximum current not to cause any damage at the PMOS drain of the core.
2. If the core is a gate, an RC low pass filter built by a protection resistor R_p and a diode p towards V_{supply} is recommended as protection. This is
15 necessary, since in modern semiconductor processes, the gate breakdown voltage is very low. The time constant of the RC low pass filter should be around 50ps, for example. In general, the protection resistor should be as large as possible, the restrictions are given by the switching frequency and input driving capability of the circuit that provides the input signal $s(t)$ to the
20 apparatus according to the present invention.

Due to the close voltage limitations, it is recommended to have the VDD protection as close as possible to the supply node. Otherwise, the interconnect lines cause an additional voltage drop resulting in junction or gate oxide breakdown in the core.

25 The present scheme can be used to protect CMOS (complementary metal oxide semiconductor) and BiCMOS circuits (bipolar devices combined with CMOS subcircuits on a single chip), for example.

The present invention can be used in mobile phones and other devices where the RF power of an antenna is measured from time to time. The invention can also be used
30 in electricity counters, interface circuits (such as RS232) and so forth.

In the drawings and specification there has been set forth preferred embodiments of the invention and, although specific terms are used, the description

thus given uses terminology in a generic and descriptive sense only and not for purposes of limitation.